# Toward accurate clock drift modeling in WSN

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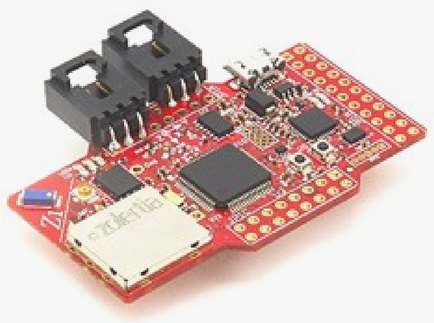
Protocols used in IoT are subject to strict temporal synchronization constraints. Time Slotted Channel-Hopping (TSCH) in particular is characterized by its very high synchronization accuracy. In this protocol synchronization errors are primarily caused by the natural clock drift observed in real nodes.



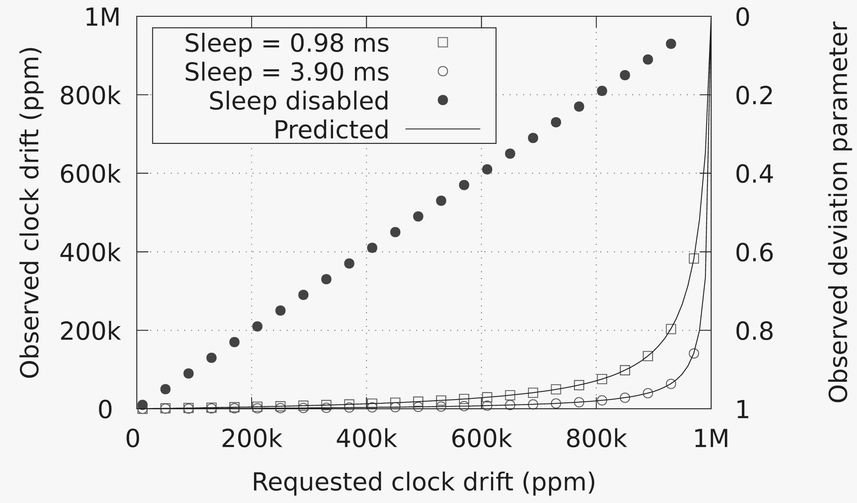
Clock frequency bias → *clock drift*
Evolves with time, temperature
Impact on MAC protocols, RDC

**WSN sensor node and crystal**

## Impact of the clock drift?

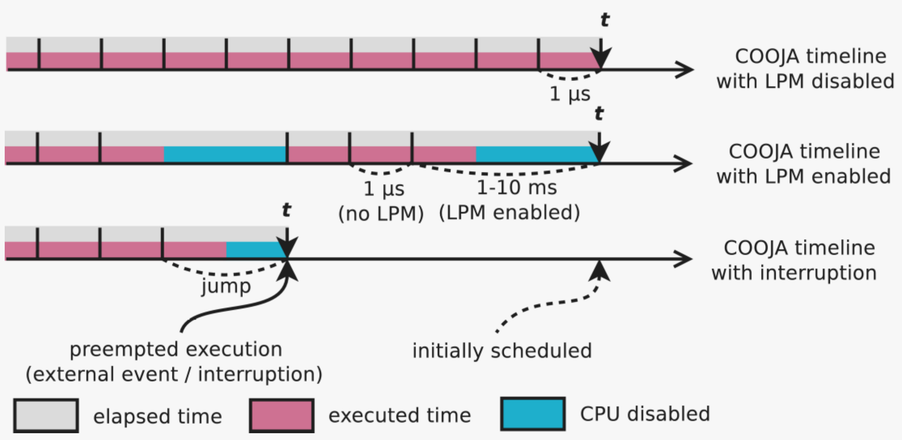
Can we model the drift in simulations?
Deviation parameter in COOJA/MSPSim

**Question: Is this approach valid?**



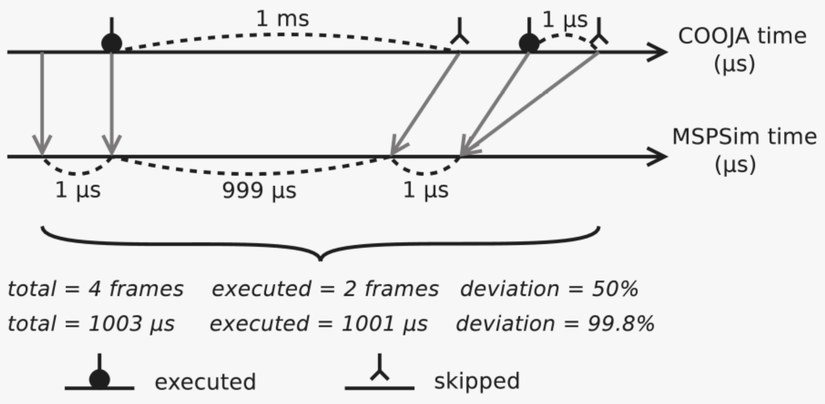

**Comparison of observed to requested deviation for MCLK**

## Simple execution model




COOJA is responsible for the advance of each mote timeline
Allow insertion of external interruption during sleep periods
Tries to jump sleep periods to accelerate simulation

## Origin of the clock drift inaccuracies




Based on frames count, not real time
Assume all execution frames have the same weight
Target deviation 50% * f, observed deviation 99.97% * f

## Predict observed inaccuracies

**Predicted deviation:**

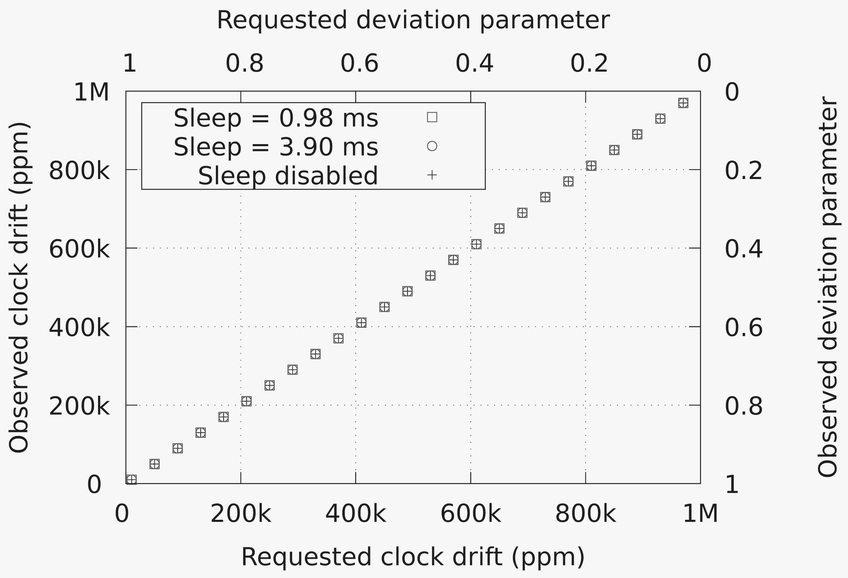
$$D(d,\alpha) = \frac{d(\alpha+1)}{d\alpha+1}$$

**Firmware characteristic:**

$$\alpha = p_s(s-1)$$

D : observed deviation
d : requested deviation
$p_s$ : probability of sleep occurrence
s : average length of sleep period

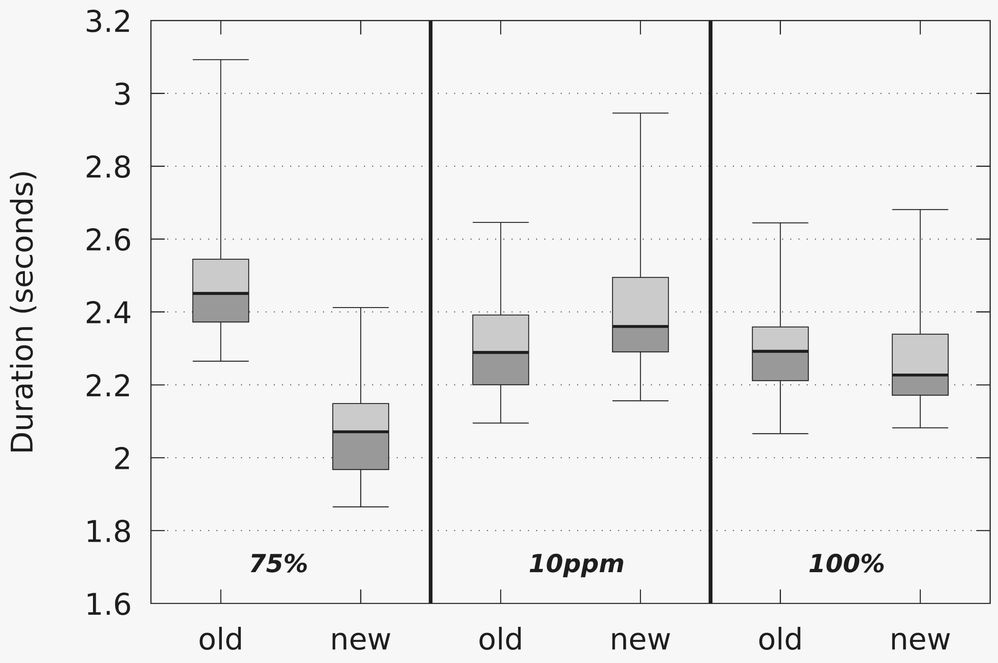
## New COOJA execution model




**Comparison of observed to requested deviation for MCLK**

Accumulate rounding error, carry on next execution frame
Works for deviation below the base frequency
Only one method to modify in COOJA

## New drift: time complexity




**Simulation duration for legacy and new drift algorithm**

Same complexity (faster in some cases)
Drift mechanism disabled when not needed



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